What is claimed is:

1. In a communication arrangement having analog circuitry and having digital signal processing circuitry clocked sufficiently fast to generate noise, the analog circuitry susceptible to processing corrupted data due to the noise coupled thereto, a method for reducing noise passed from the digital signal processing circuitry, comprising the steps of:

using the analog circuitry to capture information data from an incoming stream for at a first time interval while the digital signal processing circuitry is in a reduced-activity mode; and

in a mode other than the reduced-activity mode and during a second shorter time interval, clocking the digital signal processing circuitry to permit digital signal processing of the captured information data.

2. A method for reducing noise passed from the digital signal processing circuitry, according to claim 1, wherein the step of effectively disabling the processing of data by the analog circuitry while processing the data with the digital signal processing circuitry occurs during a known guard time for the data being communicated to the communication arrangement.

3. A method for reducing noise passed from the digital signal processing circuitry, according to claim 2, further including the step of providing both the analog circuitry and the digital signal processing circuitry on the same chip, and wherein the step of using the

analog circuitry to process data includes receiving the data in the form of low-energy data.

4. A method for reducing noise passed from the digital signal processing circuitry, according to claim 2, wherein the step of using the analog circuitry to process data includes receiving the data in the form of low-energy data and storing the data in a memory circuit.

5. A method for reducing noise passed from the digital signal processing circuitry, according to claim 4, further including inhibiting the analog circuitry from storing data in a memory circuit.

6. A method for reducing noise passed from the digital signal processing circuitry, according to claim 1, further including at least reducing power to at least one of the analog circuitry and the digital circuitry while the other circuitry is processing data.

7. A method for reducing noise passed from the digital signal processing circuitry, according to claim 1, wherein the first data-communication interval is substantially greater than the second data-communication interval.

8. A method for reducing noise passed from the digital signal processing circuitry, according to claim 1, further including providing a memory circuit in which data is

written into the memory circuit at a rate that is asynchronous to the rate at which data is read out from the memory circuit.

9. A method for reducing noise passed from the digital signal processing circuitry, according to claim 1, further including the steps of: providing a memory circuit coupled for access by at least a portion of the analogy circuitry and by at least a portion of the digital signal processing circuitry; using said at least a portion of the analog circuitry to read data out of the memory circuit and using said at least a portion of the digital signal processing circuitry to write data into the memory circuit.

10. A method for reducing noise passed from the digital signal processing circuitry, according to claim 1, further including the steps of: providing a memory circuit coupled for access by at least a portion of the analogy circuitry and by at least a portion of the digital signal processing circuitry; using said at least a portion of the analog circuitry to write data into the memory circuit and using said at least a portion of the digital signal processing circuitry to read data out of the memory circuit.

11. A communication arrangement having analog circuitry and digital signal processing circuitry, the analog circuitry susceptible to processing corrupted data due to noise coupled thereto via digital signal processing circuitry, an arrangement for reducing noise passed from the digital signal processing circuitry, comprising:

means for using the analog circuitry to process data during a first data-communication interval while the digital signal processing circuitry is in a reduced activity mode; and

means for effectively disabling the processing of data by the analog circuitry during a second shorter data-communication interval while processing the data with the digital signal processing circuitry.

12. A communication arrangement, according to claim 11, further including a single chip carrying the analog circuitry and the digital signal processing circuitry.

13. A communication arrangement, according to claim 11, further including a memory circuit arranged to store data processed by the analog circuitry while the digital signal processing circuitry is in a reduced activity mode.

14. A communication arrangement, according to claim 13, wherein the memory circuit is part of the means for using the analog circuitry to process data while the digital signal processing circuitry is in a reduced activity mode.

15. A communication arrangement, according to claim 13, wherein the memory circuit is distinct from the means for using the analog circuitry to process data while the digital signal processing circuitry is in a reduced activity mode.

16. A communication arrangement, according to claim 11, wherein the means for using the analog circuitry to process data while the digital signal processing circuitry is in a reduced activity mode includes means for receiving low-energy, high-frequency data.

17. A communication arrangement, according to claim 11, wherein the means for using the analog circuitry to process data while the digital signal processing circuitry is in a reduced activity mode includes means for transmitting data.

18. A communication arrangement susceptible to processing corrupted data due to noise coupled thereto via high-speed data processing, comprising:

a chip including both digital signal processing circuitry and analog circuitry, the digital signal processing circuitry having a reduced activity mode and a high-speed data processing mode, and the analog circuitry configured and arranged to process data during a first data-communication interval while the digital signal processing circuitry is in the reduced activity mode; and

means for effectively disabling the processing of data by the analog circuitry during a second shorter data-communication interval while processing the data with the digital signal processing circuitry.

19. A communication arrangement, according to claim 18, wherein the chip further includes the means for effectively disabling the processing of data.

20. A communication arrangement, according to claim 18, wherein digital signal processing circuitry and analog circuitry are configured and arranged to receive data.

21. A communication arrangement, according to claim 18, wherein digital signal processing circuitry and analog circuitry are configured and arranged to receive and transmit data.

22. A communication arrangement, according to claim 18, wherein both digital signal processing circuitry and analog circuitry are configured and arranged to transmit data.

23. In a communication arrangement having analog circuitry and digital signal processing circuitry, the analog circuitry coupled to receive streams of data presented thereto in the form of high-frequency signals for subsequent processing by the digital signal processing circuitry, a method for reducing noise passed from the digital signal processing circuitry to the data, comprising the steps of:

using the analog circuitry to process and to store the data during a first data-communication interval while the digital signal processing circuitry is in a reduced activity mode; and

disregarding additional data in the streams of data presented to the analog circuitry during a second shorter data-communication interval while processing the stored data with the digital signal processing circuitry.

24. In a communication arrangement having analog circuitry and digital signal processing circuitry, the analog circuitry coupled to receive streams of data presented thereto in the form of high-frequency signals for subsequent processing by the digital signal processing circuitry, a method for reducing noise passed from the digital signal processing circuitry to the data, comprising the steps of:

using the analog circuitry to process and to store the data during a first data-communication interval while the digital signal processing circuitry is in a reduced activity mode; and

disregarding additional data in the streams of data presented to the analog circuitry during a second shorter data-communication interval while processing the stored data with the digital signal processing circuitry.

25. A communication arrangement susceptible to processing corrupted data due to noise coupled thereto by high-speed data processing, comprising:

a chip including both digital signal processing circuitry and analog circuitry, the digital signal processing circuitry having a reduced activity mode and a high-speed data processing mode, and the analog circuitry configured and arranged to process data during a first data-communication interval while the digital signal processing circuitry is in the reduced activity mode; and

means for effectively disabling the processing of data by the analog circuitry during a second shorter data-communication interval while processing the data with the digital signal processing circuitry.

26. A communication arrangement, according to claim 25, wherein the analog circuitry processes data while the digital signal processing circuitry is in the reduced activity mode for at least ninety percent of a time period, and the digital signal processing circuitry processes the data for no more than the remaining portion of the time period.

27. A radio communication arrangement in which data is received using assigned frames with guard periods defined between the frames, the radio communication arrangement being susceptible to processing corrupted data due to noise coupled thereto by high-speed data processing, comprising:

a circuit including both digital signal processing circuitry and analog circuitry, the digital signal processing circuitry having a reduced activity mode and a high-speed data processing mode, and the analog circuitry configured and arranged to process data while the digital signal processing circuitry is in the reduced activity mode; and

a timer controller for causing, during the guard period, the processing of data by the analog circuitry to be effectively disabled and the digital signal processing circuitry to process the data.

28. A radio communication arrangement, according to claim 27, wherein the reduced activity mode includes at least one of: removed power to the digital signal processing circuitry; removed power to selected circuits forming part of the digital signal processing circuitry; and reduced clock speeds driving various circuits that form part of the digital signal processing circuitry.